REMARKS/ARGUMENTS

In the Office Action dated March 30, 2004, the Examiner rejected claims 1-8 as obvious over the combination of Courtright (U.S. Pat. No. 6,157,963) and Huebner. Applicant traverses the rejections of claims 1-8 and submit new claims 9-13. Based on the following arguments, Applicant submits that all pending claims are patentable.

The Examiner concluded that the following limitations from claim 1 are not disclosed in Courtright:

> **performing a contention check while executing the current process to determine whether a new client request has a transaction priority that is greater than the transaction priority of the currently client request;**
>
> **if the transaction priority of the new client request is greater than that of the current request, dispatching a process to service the new client request;**
>
> **if the transaction priority of the new request is not greater than that of the current request, determining whether the transaction priority of the current request is less than a predetermined threshold priority;**
>
> **if the transaction priority of the current client request is lower than the predetermined threshold priority and there is higher priority I/O activity present on the storage resource:**
>
> > **delaying the servicing of the current client request and forgoing the servicing of any read aheads for the current client request; and**
> >
> > **dispatching a process to service the highest priority client request that is available for service; and**
>
> **if the transaction priority of the current client request is greater than the predetermined threshold or the priority of the current client request is lower than the predetermined threshold**

and there is no higher priority I/O activity present on the storage resource:

determining whether the current client request requires any read aheads;

dispatching one or more helper processes to service any required read aheads; and

returning to the current process to service the current client request.

The Examiner, instead, turned to Huebner for allegedly teaching these limitations. Huebner is directed to a "storage device buffer access control" (see Title) that comprises a "fixed priority encoder" 58 (Figure 3). Huebner's fixed priority encoder 58 is described as follows:

> Fixed priority encoder 58 may comprise a known type of fixed priority encoder having an output 69 for signaling to memory controller 52 that access should be given to a particular client via fixed priority encoder output line 69. Fixed priority encoder 58 has a range of access request inputs 70a-70j; starting with one at its left end 70a with a higher priority and ending with input 70j at its right end having a lowest priority.
>
> ...
>
> When fixed priority encoder 58 receives a high signal at one or more of its access request inputs 70a-70j (indicating an access request) it acts on the access request corresponding to the highest priority access request input. It treats the left-most high signal level as having the highest priority, and accordingly outputs a signal on fixed priority encoder output line 69 indicating to memory controller 52 that the client corresponding to the left-most high signal level is to be granted access to memory buffer 32. In the illustrated embodiment, the highest priority client comprises a memory refresh operation which is requested via a requester signal A input to access request input 70a. When access is granted to this client, memory buffer 32 is refreshed. Memory buffer 32 is periodically refreshed under control of memory refresh timer 54, which outputs the requestor signal A.

Col. 7, lines 17-24 and 41-55.

Huebner also discloses latency controllers 76, each controller including a counter that counts "elapsing from a time at which a buffer access request was last granted to the corresponding client." Col. 8, lines 51-55. When, a latency

controller's counter expires, the priority of the corresponding client request is elevated so that the memory controller 52 will act on that the particular client request more quickly. Expiration of the counter is indicative of a client that is being "starved" for access to the memory buffer.

Huebner teaches determining when a threshold latency has been reached for a given client request and, when the threshold latency is reached, elevating the associated priority. Huebner, however, does not teach or even suggest "determining whether the transaction priority of the current request is less than a predetermined threshold priority." Huebner also does not teach or suggest performing various actions in response to determining whether a transaction priority is less than a predetermined threshold priority. For example, Huebner does not "if the transaction priority of the current client request is lower than the predetermined threshold priority and there is higher priority I/O activity present on the storage resource: delaying the servicing of the current client request and forgoing the servicing of any read aheads for the current client request; an dispatching a process to service the highest priority client request that is available for service." Huebner also does not teach or suggest that "if the transaction priority of the current client request is greater than the predetermined threshold or the priority of the current client request is lower than the predetermined threshold and there is no higher priority I/O activity present on the storage resource: determining whether the current client request requires any read aheads; dispatching one or more helper processes to service any required read aheads; and returning to the current process to service the current client request." For any or all of these reasons, Applicant submits that claim 1 and associated dependent claims are patentable over the art of record.

New claim 9 is a system claim that comprises a central processing unit ("CPU") that is configured to "to determine whether the transaction priority of the current request is less than a threshold." None of the art of record teaches this limitation nor the claimed actions that are performed by the CPU as a result of whether the transaction priority is determined to be less than the threshold. For example, the art does not teach or suggest that "if the transaction priority of the

current client request is lower than the threshold and higher priority input/output ("I/O") activity is present on a storage resource, [the CPU is adapted] to delay the servicing of the current client request and to dispatch a process to service the highest priority client request that is available for service." The art of record also is devoid of a teaching that "if the transaction priority of the current client request is greater than the threshold or the priority of the current client request is lower than the threshold and no higher priority I/O activity is present, [the CPU is configured] to determine whether the current client request requires any read aheads and to dispatch one or more helper processes to service any required read aheads." Applicant submits that claim 9 and associated dependent claim 10 are patentable over the art of record.

Claim 10 specifies that "the CPU is further configured to delay the servicing of the current request by a variable amount." Neither Huebner nor Courtright teach or suggest a variable delay. For this additional reason, claim 10 is patentable.

New claim 11 is a system claim that comprises a central processing unit ("CPU") that is configured to "to determine whether the transaction priority of the current request is less than a threshold." None of the art of record teaches this limitation nor the claimed action that is performed by the CPU as a result of whether the transaction priority is determined to be less than the threshold. The art does not teach or suggest that "if the transaction priority of the current client request is lower than the threshold and higher priority input/output ("I/O") activity is present on a storage resource, [the CPU is adapted] to delay the servicing of the current client request and to dispatch a process to service the highest priority client request that is available for service." At least for this reason, claims 11 and dependent claims 12 and 13 are patentable over the art of record.

Additionally, with regard to claim 13, the art of record is devoid of a teaching that "if the transaction priority of the current client request is greater than the threshold or the priority of the current client request is lower than the threshold and no higher priority I/O activity is present, [the CPU is configured] to determine

whether the current client request requires any read aheads and to dispatch one or more helper processes to service any required read aheads."

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,

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